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Attorney's Docket No. 67,200-409 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chen et al

Serial No. 09/ 978,420 Group No.: 2815

Filed: Oct. 15, 2001 Examiner: N. Drew Richards

For: Microelectronic Fabrication with Upper Lying Aluminum Fuse Layer in Copper Interconnect Semiconductor Technology and Method for Fabrication Thereof

Commissioner for Patents
Alexandria, VA 22313

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on Oct. 30, 2003.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

___	small entity	$165.00
X	other than a small entity	$330.00

Appeal Brief fee due: $ 330.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EL 993 945 226 US in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313

Dated: Dec. 30/03

Kathy Dixon

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 420.00	$210.00
☐	three months	$ 950.00	$475.00
☐	four months	$1,480.00	$740.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 330.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 330.00

6. FEE PAYMENT

X Attached is a Credit Card Payment Form for the sum of $ 330.00
X Credit Card Payment Form in the sum of $ 330.00 .
A duplicate copy of this transmittal is attached.

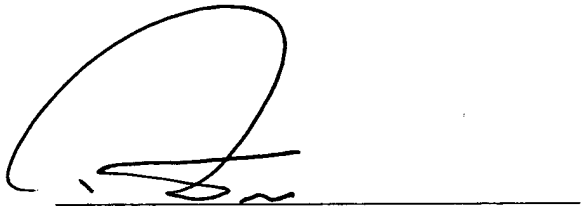
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

_X_ If any additional extension and/or fee is required, this is a request therefor to charge Deposit Account No. 50-0484

And/Or

_X_ If any additional fee for claims is required, please charge Deposit Account No. 50-0484



Signature of Attorney

Registration No. 31,311

Randy W. Tung

Telephone: (248) 540-4040

Tung & Associates
838 W. Long Lake Road, Ste. 120
Bloomfield Hills, Michigan 48302

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FROM: Tung & Associates
838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302

DATE: 30 October 2003

REF:

Appellant	:	Chen et al	Filing Date	:	15 October2001
Serial No.	:	09/978,420	Att'y No.	:	67,200-409; TSMC 00-661
Art Unit	:	2815	Examiner	:	N. Drew Richards
Title	:	Microelectronic Fabrication With Upper Lying Aluminum Fuse Layer in Copper Interconnect Semiconductor Technology and Method for Fabrication Thereof			

EXPRESS MAIL CERTIFICATE

Express Mail label Number EL 993 945 226 US
Date of Deposit ~~Nov.~~ Dec. 30, 2003

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $330.00 (required filing fee) are being deposited with the United States Postal Service via Express Mail on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313

Kathy Dixon

APPEAL BRIEF

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 30 July 2003 and made FINAL, appellant filed a notice of appeal on 30 October 2003. In accord with appellant's notice of appeal, please accept this appeal brief. No oral argument is requested.

1. Real Party in Interest

The real party in interest for this application is the assignee:

Taiwan Semiconductor Manufacturing Co., Ltd.
121 Park Avenue, No. 3
Science Based Industrial Park
Hsin-Chu, Taiwan, Republic of China

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims

Claims 1-6 and 13 are pending in this application. Claims 7-12 have been canceled. No claims have been allowed, objected to or subject to restriction. Claims 1-6 and 13 are finally rejected under 35 U.S.C. § 102(e).

4. Status of the Amendments

A reply, filed 26 September 2003, was submitted in response to the office action made FINAL, in order to overcome the Examiner's rejections of the claims pending within this application. In an advisory action mailed on 8 October 2003, the Examiner indicated that appellant's response was considered but did not place appellant's application in condition for allowance, for reasons related to those of record.

Appellant includes herewith an amendment for filing with appeal brief in accord with MPEP 1207. The amendment addresses some informalities noted by the Examiner within the office action made FINAL. The amendment is also intended to provide appellant's claims in better form for appeal. Upon entry of the amendment, claims 1-3, 6 and 13 would be pending in this application.

5. Summary of the Invention

The invention provides a microelectronic fabrication with enhanced access to a fuse layer within the microelectronic fabrication. (paragraph 0019)

The invention realizes the foregoing object by forming the fuse layer at a level no lower than a highest of a series of patterned conductor layers within the microelectronic fabrication. Thus, the fuse layer is provided with enhanced access and actuation. (paragraph 0020)

The invention is claimed in two levels of scope. Claim 1 and dependent claims 2-6 provide a method for fabricating a microelectronic fabrication where a fuse layer and the highest of the series of patterned conductor layers are formed of different conductor materials. Claim 13 provides a method for fabricating a microelectronic fabrication where a fuse layer is formed simultaneously with an alignment mark within the microelectronic fabrication.

Independent claim 13 is read on the specification and drawings as follows:

13. (previously presented) A method for fabricating a microelectronic fabrication comprising:

providing a substrate 10; (Fig. 1 and paragraph 0031)

forming over the substrate 10 a series of patterned conductor layers 14a/14b/14c/14d/14e separated by a series of dielectric layers 12; (Fig. 1 and paragraph 0031) and

forming over the substrate 10 in electrical connection with the series of patterned conductor layers 14a/14b/14c/14d/14e separated by the series of dielectric layers 12 at least one fuse layer 18b, wherein the at least one fuse layer 18b is formed at a level no lower than a highest of the series of patterned conductor layers 14a/14b/14c/14d/14e and wherein the at least one fuse layer 18b and wherein the at least one fuse layer 18b is formed simultaneously with an alignment mark 18a within the microelectronic fabrication. (Fig. 4 and paragraph 0048)

6. Issue

Whether claims 1-6 and 13 may properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Wang et al. (U.S. Pub. No. 20020155672 A1; hereinafter "Wang").

7. Grouping of Claims

Claims 1-6 (group I) are directed towards a first claimed embodiment of the invention.

Claim 13 (group II) is directed towards a second claimed embodiment of the invention.

The claims do not stand or fall together within their respective groups.

8. Argument

I. The claims do not stand or fall together within their respective groups.

With respect to group I, claims 1-6, appellant requests specific consideration of appellant's claim 4 that provides that appellant's at least one fuse layer is formed simultaneously with an alignment mark within appellant's microelectronic fabrication. In accord with further argument below, appellant asserts that at least this feature of appellant's claimed invention is novel and provides for patentability of appellant's claimed invention.

II. Claims 1-6 and 13 may not properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Wang.

a. Wang Subject Matter

Wang (Fig. 3 and paragraph 0019) discloses a microelectronic fabrication having a bond pad 112b (right hand side connected to patterned conductor layer 102) and a series of fuse layers 112b (left hand side) formed simultaneously therein.

b. The Examiner's Assertions

At page 3, last paragraph of the office action made FINAL, the Examiner asserts that Wang's fuse layer is formed simultaneously with an alignment mark within Wang's microelectronic fabrication. The Examiner apparently implicitly asserts that Wang's bond pad 112b is considered to be an alignment mark since "the passivation layer is etched aligned with the bond pad to expose the bond pad, and thus the bond pad is considered an alignment mark."

Within the advisory action continuation sheet, the Examiner further clarifies that since "the bond pad 112b of Wang has the passivation layer 118 aligned with it, thus it has been used in aligning and reads on an alignment mark."

c. Appellant's Response

Appellant notes the Examiner's foregoing assertion that Wang's bond pad 112b is an alignment mark insofar as Wang's passivation layer 118 is etched aligned with respect to Wang's bond pad 112b.

However, appellant respectfully disagrees with the Examiner's assertion since a person skilled in the art would recognize that an alignment mark within a substrate is typically employed for aligning a mask with respect to the substrate incident to use of an alignment light beam. Such is not apparently explicitly or implicitly taught within Wang. Wang at paragraph 0021 teaches the formation and patterning of Wang's passivation layer 118. However, Wang does not explicitly teach that Wang's bond pad 112b is employed as an alignment mark incident to such patterning. In addition, such is not implicit or inherent within Wang insofar as Wang may alternatively implicitly employ an alignment mark previously formed at a lower level within Wang's microelectronic fabrication for alignment of a mask for photoexposing a photoresist layer when forming a patterned photoresist etch mask layer for forming Wang's passivation layer 118. In summary, appellant is thus unable to discern that Wang explicitly, implicitly or

inherently discloses Wang's bond pad used as an alignment mark, but it is presumably implicit that a structure other than Wang's bond pad may be used as an alignment mark.

In addition, appellant also asserts that a person skilled in the art would also understand that a bond pad in plan view is generally formed in a square or rectangular shape while an alignment mark in plan view is generally formed in alternative shapes such as but not limited to cross shapes or grid shapes. Thus, bond pads and alignment marks are typically neither functionally nor geometrically equivalent.

Thus, since each and every limitation within appellant's invention as disclosed and claimed within amended claim 4 and claim 13 is not taught within Wang, in particular with respect to a fuse layer formed simultaneously with an alignment mark within a microelectronic fabrication, appellant asserts that amended claim 4 (in conjunction with base claim 1) and claim 13 may not properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Wang.

In light of the foregoing response, appellant respectfully requests that the Examiner's rejections of at least claims 4 and 13 under 35 U.S.C. § 102(e) as being unpatentable over Wang be reversed.

9. Summary

Appellant's invention as disclosed and claimed within claim 4 and claim 13 is directed towards a method for fabricating a microelectronic fabrication having formed therein a series of patterned conductor layers and a fuse layer. Within appellant's invention, the fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers. Within one aspect of the invention, the at least one fuse layer is formed simultaneously with an alignment mark within the microelectronic fabrication. Absent from the prior art of record employed in rejecting appellant's claims to appellant's invention is a disclosure of each and every limitation within appellant's invention.

10. Conclusion

Appellant requests that the Board of Patent Appeals and Interferences reverse the Examiner's action in rejecting the claims within this application within the office action made FINAL. Allowance of all claims pending within this application, in accord with the appended copy of the claims, is respectfully requested.

Respectfully submitted,

Randy W. Tung (Reg. No. 31,311)

Tung & Associates
838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302
248-540-4040 (voice)
248-540-4035 (facsimile)

APPENDIX

COMPLETE COPY OF THE CLAIMS

1. (previously presented) A method for fabricating a microelectronic fabrication comprising:

providing a substrate;

forming over the substrate a series of patterned conductor layers separated by a series of dielectric layers; and

forming over the substrate in electrical connection with the series of patterned conductor layers separated by the series of dielectric layers at least one fuse layer, wherein the at least one fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers and wherein the at least one fuse layer and the highest of the series of patterned conductor layers are formed of different conductor materials.

2. (original) The method of claim 1 wherein the microelectronic fabrication is selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. (original) The method of claim 1 wherein the at least one fuse layer is formed simultaneously with a bond pad layer within the microelectronic fabrication.

4. (original) The method of claim 1 wherein the at least one fuse layer is formed simultaneously with an alignment mark within the microelectronic fabrication.

5. (original) The method of claim 1 wherein the at least one fuse layer and the highest of the series of patterned conductor layers are formed of different conductor materials.

6. (original) The method of claim 1 wherein the at least one fuse layer is formed of an aluminum containing conductor material and the highest of the series of patterned conductor layers is formed of a copper containing conductor material.

7. - 12. (canceled)

13. (previously presented) A method for fabricating a microelectronic fabrication comprising:

providing a substrate;

forming over the substrate a series of patterned conductor layers separated by a series of dielectric layers; and

forming over the substrate in electrical connection with the series of patterned conductor layers separated by the series of dielectric layers at least one fuse layer, wherein the at least one fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers and wherein the at least one fuse layer and wherein the at least one fuse layer is formed simultaneously with an alignment mark within the microelectronic fabrication.